Application of Mass Metrology in Advanced Device Manufacture

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Abstract:

Mass metrology is an innovative technique used to monitor processes in advanced semiconductor device manufacturing. Accurate measurement of the mass change in the process step allows determination of parameters such as thickness (or etch depth), density, and composition \cite{1}. Measuring on-product wafers, the methodology provides a fingerprint of the process, enabling in-line production monitoring and control.

Production applications where mass metrology can be used include both removal steps; wet etch, plasma etch and CMP processes, as well as critical deposition steps; such as low-k and high-k materials, atomic layer deposition, and multiayer stacks of dielectric or metals.

This paper will explain the concept and principles of mass metrology, outlining specific case studies in both front end of line (FEoL) and back end of line (BEoL) processes.

FEOL processes include Silicon etch (STI and Deep Trench) and a range of applications in the creation of the gate structure; monitoring of strained gates, High-k materials, and metal gates.

BEOL Interconnect applications focus on the advanced thin barrier layers and stacks which challenge existing metrology techniques. BEoL IMD applications include monitoring advanced Low k materials, with Curing, Plasma Damage and Low-k Restoring all monitored effectively using mass.

Experimental:

Mass metrology is founded on the principle that all devices are manufactured through process steps, each adding or removing material. All results for applications reviewed are based on before process and after process measurements, accurately reporting the mass change ($\Delta$Mass) due to process. The Mentor system measures each 300mm or 200 mm wafer in approximately 1min, including the robotic handling from a FOUP, SMIF or cassette. The resolution of the reported mass is 10µg, with a 1σ dynamic repeatability error of <0.08mg. This error corresponds to thickness values on a 300mm wafer as <5Å of SiO$_2$ or ~1Å of a denser material such as TaN.

FEOL – Shallow Trench Isolation

The STI module incorporates a number of process steps: pad oxide/nitride stack deposition, photolith, dry etching, ashing and wet strip, cavity HF dip for corner rounding, clean and liner oxidation, HARP oxide deposition, field oxide recess, chemical mechanical polishing and finally nitride removal; all process where mass metrology may be applied \cite{2}.

Characterisation of the STI etch and strip process in particular has highlighted process variability due to post-etch residues. In monitoring a batch of 24 wafers, the mass fingerprint of STI etch and strip is Si removal of $\sim$51.5mg.

In Figure 1, it can be seen that mass loss on the first 10 wafers is significantly lower than the rest, and this is explained by an excess post-etch residue.

![Fig.1 STI Etch & Strip Process](image-url)
The excessive residue adversely affects the final STI structure, where the desired top corner rounding is not achieved in the HF Dip.

**FEOL – Silicon Deep Trench**

High-aspect ratio etched features in silicon, such as the Deep Trench (DT) capacitor are a challenge for current metrology techniques. The measured mass change is responsive to CD, aspect ratio, or etch polymers, and is independent of the underlying material; a direct representation of the process result. In this case, the ΔMass provides reliable information on the average DT volume [3]. This information is then used in a feed-forward methodology to control the subsequent mask and bottle etch process, thus defining the capacitor performance.

**FEOL – Silicon Nitride – Strained Gate fabrication**

The use of a Strained Silicon Nitride Contact Etch Stop Layer (CESL) is key to enhancing the functional performance in advanced devices. A repeatable, controlled silicon nitride stress is essential. Data shows that the stress of silicon nitride is related to composition (Si:N ratio)[4], which may be monitored by density (mass). Mass metrology is capable of measuring approximately 2Å (1σ) changes in the thickness of Silicon Nitride and 0.05g/cm3 in density changes.

**FEOL – High-k / Metal gate fabrication**

Monitoring the Silicon content in Hf\(_x\)Si\(_y\)O is crucial to ensure the gate dielectric performance. Mass metrology allows calculation of the gate material density, which relates directly to the ratio of Hf:S content in the film.

Mass metrology has been successfully correlated to RBS using blanket films, as RBS is not suitable for production. Figure 3 shows the excellent agreement between silicon content and film density. Mass measurement, effective at a target thickness of only 200Å, exhibits an error of just 0.5 at% which is also better than the 2.0 at% reported by RBS.

**BEoL – Low-k Films**

Low-k dielectric films are increasingly used in advanced technology nodes. Mass as a metrology technique is well suited, due to the fundamental relationship between density and k-value, represented by the Clausius-Mosotti equation. Monitoring of density changes, measured to an accuracy of 0.01g/cm\(^3\), provides a quick, reliable method for recognizing changes in dielectric constant. [5]
Increased porosity of Low-k films is creating certain integration issues, as the material may be damaged by etch or resist strip processes. Mass metrology offers a simple and direct method to monitor moisture absorption due to plasma damage. Figure 5 shows the percentage increase in the film’s mass as a function of time exposure to the Fab ambient. The film mass increased nearly 2% (on ave.) in a 2-week period, with half (~0.2mg mass change) occurring in the first 72 hrs.

**Ambient Moisture Uptake**

<table>
<thead>
<tr>
<th>% Mass Increase</th>
<th>Time Exposed</th>
</tr>
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<tbody>
<tr>
<td>0%</td>
<td>0 hrs</td>
</tr>
<tr>
<td>0%</td>
<td>24 hrs</td>
</tr>
<tr>
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<td>72 hrs</td>
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<td>0%</td>
<td>1 week</td>
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<tr>
<td>0%</td>
<td>2 weeks</td>
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**Fig.5 Mass change monitoring of Low-k damage**

Mass metrology, a non-destructive technique that directly monitors product wafers, distinguishes quantitative differences in plasma damage; thereby enabling rapid and efficient process optimization. It can be extended to evaluating the restoration process, ensuring the Low-k process module is well controlled.

**BEoL – Barrier layers**

Implementation of Cu interconnect technology requires thin barrier layers to restrict interdiffusion and improve electromigration performance. The atomic level accuracy of the mass response provides a unique metrology solution in the characterization of ultra-thin ALD liners and cap films.

Electroless deposition of CoWP is a sequential process including a CuO clean, followed by the CoWP deposition. Maintaining the optimised CoWP solution is challenging, and therefore directly impacts the process repeatability. Mass monitoring of the deposition on product wafers provides a confirmation of a satisfactory result.

In Figure 6, the pairing with a thickness measurement (reflectometry), shows a unique capability to monitor the effectiveness of the CuO clean step [6]. Variance in the CuO pre-clean, or micro-loading of the CoWP both result in measurable mass changes, and are detected as undesirable process excursions.

**Conclusion**

Mass metrology provides key advantages in production operations by monitoring process performance independent of substrate, wafer size, type, and material. The methodology is applicable across the full spectrum of process technologies. Implementation of mass metrology does not require complex characterization or models that assume fixed input parameters to produce the output parameter. Mass measurement offers a high wafer throughput and low cost-of-ownership, allowing manufacturers to realize Stop-Go process affirmation, detect process drift, and carry out Feed-Forward process controls.

**References**


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